

REMARKS

Claims 1-3 and 5 are pending in the instant application. In view of the following remarks, favorable reconsideration of this case is respectfully requested.

Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent No. 5,889,314 to Hirabayashi (hereinafter referred to as Hirabayashi). Applicants respectfully traverse.

Claim 1 relates to a semiconductor integrated circuit that includes, *inter alia*, a silicon epitaxial layer that touches the surface of said silicon substrate and has ***a lower resistivity than the resistivity of said silicon substrate.***

The Examiner asserts that Hirabayashi discloses a semiconductor integrated circuit as recited in claim 1. In particular, the Examiner asserts that Hirabayashi discloses a silicon epitaxial layer that touches the surface of said silicon substrate and has a lower resistivity than the resistivity of said silicon substrate. (Office Action; page 2, lines 9-11). However, the cited section of Hirabayashi states in its entirety “p-type silicon substrate containing a high concentration of p-type impurity and thus exhibiting ***a low electrical resistance***”. (Hirabayashi; col. 1, lines 61-63; emphasis added). Therefore, p-well of layer 22 of Hirobayashi does not necessarily have a lower resistivity than p-type substrate 20. In fact, Hirobayashi indicates that p-type silicon substrate 20 has ***a low electrical resistance***. (Hirobayashi; col. 1, lines 61-63). Therefore, since the substrate of Hirabayashi has a low electrical resistance, Hirabayashi does not disclose or suggest an epitaxial silicon layer having a lower resistivity than the silicon substrate. Therefore, Hirabayashi does not disclose or suggest this feature of claim 1, and for at least this reason claim 1 is allowable.

Claim 5 depends from claim 1 and is therefore allowable for at least the same reasons as claim 1 is allowable.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirabayashi. Applicants respectfully traverse.

Claim 2 and 3 depend from claim 1 and are therefore allowable for at least the same reasons as claim 1 is allowable.

Additionally, claim 2 recites that the resistivity of said silicon substrate is between 20 and 100 times the resistivity of said silicon epitaxial layer, and claim 3 recites that the resistivity of said silicon substrate is between 50 and 100 times the resistivity of said silicon epitaxial layer. The Office Action rejects these claims as obvious by stating that the adjustment of the ranges claimed would be obvious. However, the criticality of the dimensions recited in claims 2 and 3 is supported in figure 4 of the specification. Figure 4 is a graph showing the effect that the resistivity of the support substrate causes to the noise propagation by taking the resistivity of support substrate on the axis of abscissas and propagation characteristic of the noise in the support substrate on the axis of ordinates. The specification discusses figure 4 at page 12, line 11, to page 13, line 17. In particular, the specification states that figure 4 shows "the noise propagation quantity between the P-type diffusion layers reduced as the resistivity of the P-type bulk substrate as the support substrate became higher." (Specification; page 13, lines 7-10). Therefore, the criticality of the stated resistivity ratios are supported in the specification and figures, and it is therefore respectfully submitted that claims 2 and 3 are allowable over the reference.

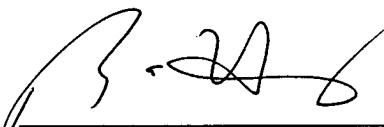
An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that independent claim 1 is in

condition for allowance, as well as those claims dependent therefrom. Passage of this case to allowance is earnestly solicited.

However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged on Deposit Account 50-1290.

Respectfully submitted,



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